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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,115	06/18/2004	Ram Kelkar	BUR920040047US1	4114

29371 7590 08/26/2005

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EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H'D

Office Action Summary	Application No.	Applicant(s)	
	10/710,115	KELKAR ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,12,13,16 and 17* is/are rejected.

7)☒ Claim(s) *3,4,7-11,14,15 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2004* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *06/18/04, 07/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-18 are presented in the instant application according to the Applicants' filing on 06/18/2004.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-2, 5-6, 12-13 and 16-17 are rejected under 35 U.S.C. 102(e) as being as being anticipated by Chen (U.S. Pub. No. 2005/0088210).

With respect to claims 1 and 12, Chen discloses, in Fig. 1, a digital frequency divider apparatus comprising a plurality of next-state generator elements [left flip-flops in boxes 14 and 16] receiving an input clock signal [CLK0] thereto, and configured to generate a next value for each of a corresponding plurality of internal state variables, a plurality of flip-flop elements [right flip-flops in boxes 14 and 16] configured to store the generated next values for the plurality of internal state variables, and the plurality of flip-flop elements further configured to provide a present value of the plurality of internal state variables to the next-state generator elements through a feedback path there between [from right flip-flops to left flip-flops], in which the generated next values for the plurality of internal state variables are based upon the present values of the plurality of internal state variables and the input clock signal [CLK0].

With respect to claims 2 and 13, Chen further discloses, in Fig. 1, a reset element [Reset] associated with each of the next-state generator elements, the reset element configured for setting the internal state variables and their complements to a desired initial value.

With respect to claims 5 and 16, Chen inherently discloses, in Fig. 1, that the next-state generator elements [left flip-flops in boxes 14 and 16] are implemented with CMOS logic.

With respect to claims 6, 12 and 17, Chen discloses, in Fig. 1, a digital frequency divided by N divider apparatus, comprising a plurality of next-state generator elements [left flip-flops in boxes 14 and 16] receiving an input clock signal [CLK0] thereto, and configured to generate a next value for each of a corresponding plurality of internal state variables, a plurality of flip-flop

elements [right flip-flops in boxes 14 and 16] configured to store the generated next values for plurality of internal state variables, the plurality of flip-flop elements further configured to provide a present value of the plurality of internal state variables to the next-state generator elements through a feedback path there between, the generated next values for the plurality of internal state variables based upon the present values of the plurality of internal state variables and the input clock signal; and one or more of the next-state generator elements further configured to generate a preactivated internal state variable prior to a transition from state X to state X+ 1, during the transition at least one of the internal state variable changes, and at least one of the next value also changes as a result thereof.

Allowable Subject Matter

4. Claims 3-4, 7-11, 14-15 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

a) The frequency divider apparatus, in which the flip-flop elements further includes double edge triggered, D flip-flop elements, as called for in claims 3 and 14;

b) The frequency divider apparatus, in which one or more of the next-state generator elements configured to generate a preactivated internal state variable further comprises logic configured to detect state X; a latch mechanism coupled to an output of the logic, the latch mechanism configured to precharge a transistor device such that a preactivated internal state

variable is realized immediately upon a change in the input clock signal at state X+ 1, as called for in claims 7 and 18;

Citation of Relevant Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Kouznetsov et al. (U.S. Patent No. 6,501,816) discloses a fully programmable multimodulus prescaler.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER